REMARKS/ARGUMENTS

Claims 1-29 are pending. Claims 1, 7-10, 13-15, 18, and 24 have been amended. New claims 25-29 have been added. No new matter has been introduced.

Applicant notes with appreciation the indicated allowability of claims 16, 17, 19, 20, and 23. These claims have been rewritten as new claims 25-29. Accordingly, claims 25-29 are allowable.

Claims 1-4, 6, and 8-12 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Handy "The Cache Memory Handbook." Claims 1, 5, 7, 14, 15, and 18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Gannon et al. (USP 5,265,232). Claims 13 and 24 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Bauman (USP 6,480,927).

Applicant respectfully submits that independent claim 1 is novel and patentable over Handy and Gannon et al. because, for instance, they do not teach or suggest storing copies of address tags stored in the plurality of caches in a cache directory which has at least one entry each including a plurality of bits, wherein the bits of each entry in the cache directory are divided into a plurality of parts; and processing a plurality of search requests concurrently using the plurality of parts. Handy (p. 55) and Gannon et al. (Fig. 11) disclose ordinary multi-way set associative type cache wherein the whole of the directory is divided into a plurality of parts. In contrast, claim 1 recites that the bits of each entry in the directory are divided into a plurality of parts (e.g., one part comprises even bits of the entry and the other part comprises odd bits of the entry). Accordingly, a plurality of search requests for the directory may be processed concurrently.

For at least the foregoing reasons, claim 1 and claims 2-6 depending therefrom are novel and patentable.

Applicant respectfully asserts that independent claim 7 is novel and patentable over Gannon et al. because, for instance, Gannon et al. does not disclose or suggest a cache directory storing copies of address tags associated with the cache storage module, wherein each copy of address tag includes a plurality of bits, the bits of each copy of address tag of the cache

directory is divided into a plurality of units capable of operating in parallel, and a coherence control device processes a plurality of search requests concurrently using the plurality of units. As discussed above, Gannon et al. merely discloses dividing the whole of the directory into parts.

Applicant respectfully contends that independent claim 8 is novel and patentable over Handy because, for instance, Handy does not teach or suggest partitioning the bits of a search request address tag into a first plurality of sections, partitioning the bits of each address tag of a plurality of address tags in the cache directory into a second plurality of sections, and comparing for each address tag, a first section of the first plurality of sections with a first section of the second plurality of sections. As discussed above, Handy merely discloses dividing the whole of the directory into parts.

For at least the foregoing reasons, claim 8 and claim 9 depending therefrom are novel and patentable.

Applicant respectfully submits that independent claim 10 is novel and patentable over Handy because, for instance, Handy does not disclose or suggest selecting a section of the plurality of sections associated with the memory bank, wherein the bits of each section in said cache directory are divided into a plurality of parts, and searching the section for the write request address using the plurality of parts. As discussed above, Handy merely discloses dividing the whole of the directory into parts.

For at least the foregoing reasons, claim 10 and claims 11-12 depending therefrom are novel and patentable.

Applicant respectfully asserts that independent claim 13 is novel and patentable over Bauman because, for instance, Bauman does not teach or suggest a crossbar switch for coupling the input module with the plurality of sub-directories, each subdirectory including at least one entry having a plurality of bits, wherein the bits of each entry are divided into a plurality of parts; and a control module for routing a first request of the plurality of requests to a first subdirectory of the plurality of sub-directories and a second request of the plurality of requests to a second subdirectory of the plurality of sub-directories for concurrent searching of the first and second subdirectories using the plurality of parts, when the first and second requests address different memory banks of the plurality of memory banks. Bauman merely discloses

ordinary multi-way set associative type cache wherein the whole of the directory is divided into a plurality of parts (Figs. 5 and 6).

Applicant respectfully contends that independent claim 14 is novel and patentable over Gannon et al. because, for instance, Gannon et al. does not teach or suggest partitioning the bits of each entry in the cache directory into a plurality of parts, wherein each part of the plurality of parts is searched concurrently with another part of the plurality of parts. As discussed above, Gannon et al. merely discloses dividing the whole of the directory into parts.

For at least the foregoing reasons, claim 14 and claims 15-17 depending therefrom are novel and patentable.

Applicant respectfully submits that independent claim 18 is novel and patentable over Gannon et al. because, for instance, Gannon et al. does not disclose or suggest a cache directory comprising copies of address tags stored in a plurality of caches, each copy of address tag having a plurality of bits, wherein the bits of each copy of address tag in the cache directory are divided into a plurality of parts; and a plurality of units for processing a plurality of search requests concurrently using the plurality of parts. As discussed above, Gannon et al. merely discloses dividing the whole of the directory into parts.

For at least the foregoing reasons, claim 18 and claims 19-22 depending therefrom are novel and patentable.

Applicant respectfully asserts that independent claim 24 is novel and patentable over Bauman because, for instance, Bauman does not teach or suggest an input module configured to receive a write request address by the cache directory from another processor, wherein the bits of each section in the cache directory are divided into a plurality of parts; and a comparison module configured to search the section for the write request address using the plurality of parts. As discussed above, Bauman merely discloses dividing the whole of the directory into parts.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

Chun-Pok Leung
Reg. No. 41,405

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300

Attachments
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